

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

NVIDP486/P003259

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Application Number

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First Named Inventor

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Art Unit

2188

Examiner

Walter, Craig E.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)☒ attorney or agent of record. 41,429
Registration number _____☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____/KEVINZILKA/

Signature

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Telephone number

June 26, 2007

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.☒ *Total of 1 forms are submitted.

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REMARKS

The Examiner has rejected Claim 31 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner has argued that ‘one of ordinary skill in the art would not understand how an asserted signal (i.e. strobe) itself can be “coupled to [a memory]”’ and that “one skilled in the art would recognize that only a physical medium itself, carrying said signal could be coupled to the memory.” Applicant respectfully disagrees and asserts that “asserting a common write strobe coupled to all of the FIFO memories” does in fact comply with the enablement requirement.

In addition, the Examiner has rejected Claims 12 and 17-25 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner has argued that ‘the phrase “on the fly” renders the claim indefinite.’ Applicant respectfully disagrees and notes that the above claim language is to be read according to the plain and ordinary meaning thereof, in view of relevant dictionary definitions, and in further view of the definitions provided in the specification, as noted in the Amendment dated 01/15/2007.

The Examiner has rejected Claims 1, 3-5, 8, 10-12, 14, 16, 26-28, and 31 under 35 U.S.C. 102(b) as being anticipated by Searby (U.S. Patent No. 5,765,186). Additionally, the Examiner has rejected Claim 15 under 35 U.S.C. 103(a) as being unpatentable over Searby, in view of Official Notice. Further still, the Examiner has rejected Claims 2, 9, 17, and 19-25 under 35 U.S.C. 103(a) as being unpatentable over Searby, in view of Stolowitz (U.S. Patent No. 6,018,778). Applicant respectfully disagrees with such rejections.

With respect to independent Claims 1 and 10, the Examiner has relied on Col. 3, lines 52-67 from the Searby reference to make a prior art showing of applicant’s claimed “receiving and storing read data responsive to timing signals provided by the respective

drive” (see this or similar, but not necessarily identical language in the aforementioned claims). Applicant’s arguments made on page 12 of the Amendment mailed 01/15/2007 are hereby incorporated by reference.

In the Office Action dated 03/26/2007, the Examiner has argued that “[a]pplicant does in fact describe synchronizing the data transfer from drives to the buffer” and has further argued that “[a]pplicant concedes by his own admission that Searby synchronizes data transfer from the drives to the RAM buffer, as similarly recited by [a]pplicant in the preamble.”

Applicant respectfully disagrees and notes that applicant claims “receiving and storing read data responsive to timing signals provided by the respective drive” (emphasis added), in the context claimed. In addition, the excerpts relied on by the Examiner merely teach “transferring means comprising means for providing an indication when said data is available for transfer” and that “the controlling means [are] responsive to said indication from said transferring means” (Col. 3, line 59 – Col. 4, line 1 – emphasis added). However, merely disclosing controlling means responsive to an indication from a transferring means that data is available for transfer, as in Searby, does not teach “receiving and storing read data responsive to timing signals provided by the respective drive” (emphasis added), as claimed by applicant. Clearly, an indication from transferring means, as in Searby, simply fails to even suggest “timing signals provided by the respective drive” (emphasis added), in the manner as claimed by applicant.

In addition, with respect to independent Claims 1 and 10, the Examiner has relied on Col. 5, lines 38-49 from the Searby reference to make a prior art showing of applicant’s claimed “causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive” (see this or similar, but not necessarily identical language in the aforementioned claims). Applicant’s arguments made on page 12, last paragraph, through page 13, first paragraph of the Amendment mailed 01/15/2007 are hereby incorporated by reference.

In the Office Action dated 03/26/2007, the Examiner has argued that in “Searby in Fig. 2, and col. 5, lines 39-49, a request signal is associated with each respective drive, in order to control the transfer of information.” Applicant respectfully disagrees and notes that the excerpts relied on by the Examiner merely teach that “a system controller... receives frame request data from an external processing apparatus... via request bus 52 and in response thereto outputs control data” (Col. 5, lines 39-42 – emphasis added). In addition, Searby teaches that “[t]he controller 51 also receives request signals REQ from each of the second SCSI interfaces... associated with the RAM buffers... thereby controlling the outputting of data” (Col. 5, lines 44-49 – emphasis added). However, receiving request signals which control the output of data, as in Searby, does not teach “causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive” (emphasis added), as claimed by applicant. Clearly, receiving request signals from each of the second SCSI interfaces, as in Searby, simply fails to even suggest “timing signals provided by the respective drive” (emphasis added), in the manner as claimed by applicant.

Further, with respect to independent Claims 1, and 10, the Examiner has relied on Fig. 2, element 49 and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of applicant’s claimed “monitoring each of the two-port memories to detect a non-empty condition” (see this or similar, but not necessarily identical language in the aforementioned claims). Applicant’s arguments made on page 13, second paragraph, through page 14, first paragraph of the Amendment mailed 01/15/2007 are hereby incorporated by reference.

In the Office Action dated 03/26/2007, the Examiner has relied on an inherency argument regarding applicant’s claimed “monitoring each of the two-port memories to detect a non-empty condition,” as claimed. Specifically, the Examiner has argued that “memory monitoring to some degree is inherent in a system such as Searby’s... since Searby’s system is directed to the parallel transfer of data, the system must wait until

each of the memories has data present before the data can be sent to the highway” and that therefore, “his system must inherently perform some sort of monitoring process of the memories to determine if data is present to transfer.”

Applicant respectfully disagrees and asserts that Searby merely discloses that “[t]he registers 41 to 44 each hold a single word of data and the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence” and that “[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49” (Col. 7, lines 39-42 – emphasis added). However, merely enabling a tri-state buffer for output of the data word from the respective register, as in Searby, simply fails to even suggest “monitoring each of the two-port memories to detect a non-empty condition” (emphasis added), as claimed. In view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested. (See MPEP 2112)

Further, with respect to independent Claims 1, 10, and 17, the Examiner has relied on Fig. 2, elements 49 and 50; Col. 5, lines 22-37; Col. 6, lines 14-31; and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of applicant’s claimed “synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer” (see this or similar, but not necessarily identical language in the aforementioned claims). Applicant’s arguments made on page 14, second paragraph, through page 14, last paragraph of the Amendment mailed 01/15/2007 are hereby incorporated by reference.

In the Office Action dated 03/26/2007, the Examiner has argued that ‘synchronous data is formed and written at least by the time it is transmitted, hence Searby does in fact [teach] “synchronously reading the transferred data from all of the two-port memories”’ and that “therefore the data *formed* from this transmission is in fact synchronous as required by the instant claim.” Applicant respectfully disagrees and notes that the excerpts from Searby relied on by the Examiner merely teach that “[o]nce all of

the data for the requested frame has been transferred to the RAM buffers... it can be output therefrom to the highway” (Col. 7, lines 32-34) where “the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence” and that “[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49” (Col. 7, lines 40-42 — emphasis added). However, the mere disclosure that the word is output as each tri-state buffer is enabled in sequence and individually output from the register to the highway, as in Searby, simply fails to even suggest “forming synchronous read data” by “synchronously reading the transferred data from all of the two-port memories” (emphasis added), as claimed by applicant.

Further, with respect to independent Claim 26, the Examiner has relied on Fig. 2, element 49 and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of applicant’s claimed “monitoring each of the two-port memories to detect a non-full condition.”

Applicant respectfully notes that the excerpts from Searby relied on by the Examiner merely teach that “[o]nce all of the data for the requested frame has been transferred to the RAM buffers... it can be output therefrom to the highway” (Col. 7, lines 32-34). However, merely teaching that data for a requested frame is output from the RAM buffers once its has all been transferred, as in Searby, does not teach “monitoring each of the two-port memories to detect a **non-full** condition” (emphasis added), as claimed by applicant.

Thus, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.